

Dear IP Professional,

This document contains a list of issued patents and pending patent applications assigned to Ternarylogic LLC of Morristown, NJ as of December 28, 2017. The status of the portfolio still changes as the USPTO continues to allow and issue patents in the portfolio and new applications are filed.

A copy of this document can be downloaded from [www.ternarylogic.com/portfolio.pdf](http://www.ternarylogic.com/portfolio.pdf). The document has live links to the USPTO database to make review easier.

Those who want to obtain a patent or application in PDF format are referred to [www.pat2pdf.org](http://www.pat2pdf.org) which allows downloading a patent or patent application in PDF format. Just enter the patent or patent publication number into the search window.

Many applications are still alive, even after issuance, by filing of continuations and continuations-in-part. Please, check USPTO PAIR for case histories.

This document is provided “as is” for your review. Please, contact us at [admin@ternarylogic.com](mailto:admin@ternarylogic.com) if you are interested in obtaining a license. Please note that some patents contain errors in the claims. Some claims wrongly exclude binary configurations. It is strictly the reader’s responsibility to decide if a claim is infringed. Please check a patent’s case history in PAIR when in doubt.

### **The subject matter of the portfolio**

The subject matter of the portfolio is related to non-binary switching and applications thereof. The portfolio covers a range of subjects that includes:

- basic components such as n-state switches, inverters and memories;
- non-binary and binary Linear Feedback Shift Register applications;
- binary and non-binary self synchronizing scramblers/descramblers;
- machine arithmetic;
- encryption;
- error-correction methods and apparatus;
- secure unlocking of devices; and
- cryptographic applications.

### **How to access the portfolio**

Please click on a specific patent number or patent application number to open a related web site at the U.S. Patent and Trademark Office (USPTO).

### **Contact us**

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**Issued patents**

46	<a href="#">9,298,423</a>	Methods and systems for determining characteristics of a sequence of n-state symbols
45	<a href="#">9,218,158</a>	N-Valued Shift Registers with Inverter Reduced Feedback Logic Functions
44	<a href="#">9,203,438</a>	Error correction by symbol reconstruction in binary and multi-valued cyclic codes
43	<a href="#">9,203,436</a>	Error correction in multi-valued (p,k) codes
42	<a href="#">9,100,166</a>	Method and apparatus for rapid synchronization of shift register related symbol sequences
41	<a href="#">8,832,523</a>	Multi-state symbol error correction in matrix based codes
40	<a href="#">8,817,928</a>	Method and apparatus for rapid synchronization of shift register related symbol sequences
39	<a href="#">8,645,803</a>	Methods and systems for rapid error correction by forward and reverse determination of coding states
38	<a href="#">8,589,466</a>	Ternary and multi-value digital signal scramblers, descramblers and sequence generators
37	<a href="#">8,577,026</a>	Methods and apparatus in alternate finite field based coders and decoders
36	<a href="#">8,374,289</a>	Generation and detection of non-binary digital sequences
35	<a href="#">8,364,977</a>	Methods and systems for processing of n-state symbols with XOR and EQUALITY binary functions
34	<a href="#">8,345,873</a>	Methods and systems for N-state signal processing with binary devices
33	<a href="#">8,225,147</a>	Multi-valued scrambling and descrambling of digital data on optical disks and other storage media
32	<a href="#">8,209,370</a>	Multi-value digital calculating circuits, including multipliers
31	<a href="#">8,201,060</a>	Methods and systems for rapid error correction of Reed-Solomon codes
30	<a href="#">8,180,817</a>	Encipherment of digital sequences by reversible transposition methods
29	<a href="#">8,149,143</a>	Data encryption and decryption with a key by an N-state inverter modified switching function
28	<a href="#">8,103,943</a>	Symbol reconstruction in Reed-Solomon codes
27	<a href="#">8,046,661</a>	Symbol error correction by error detection and logic based symbol reconstruction
26	<a href="#">7,930,331</a>	Encipherment of digital sequences by reversible transposition methods
25	<a href="#">7,924,176</a>	N-state ripple adder scheme coding with corresponding N-state ripple adder scheme decoding
24	<a href="#">7,877,670</a>	Error correcting decoding for convolutional and recursive systematic convolutional encoded sequences
23	<a href="#">7,865,807</a>	Multi-valued check symbol calculation in error detection and correction
22	<a href="#">7,865,806</a>	Methods and apparatus in finite field polynomial implementations

21	<a href="#">7,864,087</a>	Methods and systems for modifying the statistical distribution of symbols in a coded message
20	<a href="#">7,864,079</a>	Ternary and higher multi-value digital scramblers/descramblers
19	<a href="#">7,782,089</a>	Multi-state latches from n-state reversible inverters
18	<a href="#">7,772,999</a>	N-state ripple adder scheme coding with corresponding n-state ripple adder scheme decoding
17	<a href="#">7,725,779</a>	Multi-valued scrambling and descrambling of digital data on optical disks and other storage media
16	<a href="#">7,696,785</a>	Implementing logic functions with non-magnitude based physical phenomena
15	<a href="#">7,659,839</a>	Methods and systems for modifying the statistical distribution of symbols in a coded message
14	<a href="#">7,656,196</a>	Multi-state latches from n-state reversible inverters
13	<a href="#">7,643,632</a>	Ternary and multi-value digital signal scramblers, descramblers and sequence generators
12	<a href="#">7,580,472</a>	Generation and detection of non-binary digital sequences
11	<a href="#">7,562,106</a>	Multi-value digital calculating circuits, including multipliers
10	<a href="#">7,548,092</a>	Implementing logic functions with non-magnitude based physical phenomena
9	<a href="#">7,505,589</a>	Ternary and higher multi-value digital scramblers/descramblers
8	<a href="#">7,487,194</a>	Binary and n-valued LFSR and LFCSR based scramblers, descramblers, sequence generators and detectors in Galois configuration
7	<a href="#">7,397,690</a>	Multi-valued digital information retaining elements and memory devices
6	<a href="#">7,365,576</a>	Binary digital latches not using only NAND or NOR circuits
5	<a href="#">7,355,444</a>	Single and composite binary and multi-valued logic functions from gates and inverters
4	<a href="#">7,277,030</a>	Sequence detection by multi-valued coding and creation of multi-code sequences
3	<a href="#">7,218,144</a>	Single and composite binary and multi-valued logic functions from gates and inverters
2	<a href="#">7,064,684</a>	Sequence detection by multi-valued coding and creation of multi-code sequences
1	<a href="#">7,002,490</a>	Ternary and higher multi-value digital scramblers/descramblers

One is cautioned that the issued patents cover inventions as provided in the claims. The title of a patent may refer to a parent patent of which it is a continuation. Furthermore, claims in an issued patent may have mistakes that are corrected by a Certificate of Correction. Furthermore, additional aspects may be claimed in continuation applications that have not yet been issued. Please review a patent's case history in the USPTO PAIR website for details.

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## **PUBLISHED Patent Applications**

Provisional Appl.	Lab-transformed Cryptographic Machines and Methods
<a href="#">20170230509</a>	Method and Apparatus for Wirelessly Activating a Remote Mechanism
<a href="#">20170169735</a>	Cryptographic Machines With N-state Lab-transformed Switching Devices
<a href="#">20160366109</a>	Method and Apparatus for Validating a Transaction between a Plurality of Machines
<a href="#">20160211971</a>	Apparatus for Unconventional Non-Linear Feedback Shift Registers (NLFSRs)
<a href="#">20160112069</a>	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders
<a href="#">20150310680</a>	Method and Apparatus for Wirelessly Activating a Remote Mechanism
<a href="#">20150160922</a>	N-Valued Shift Registers with Inverter Reduced Feedback Logic Functions
<a href="#">20140321585</a>	Method and Apparatus for Rapid Synchronization of Shift Register Related Symbol Sequences
<a href="#">20140281761</a>	Reversible corruption of a digital medium stream by multi-valued modification in accordance with an automatically generated mask
<a href="#">20140055290</a>	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders
<a href="#">20140032623</a>	Methods and Systems for Determining Characteristics of a Sequence of n-state Symbols
<a href="#">20130230172</a>	Novel binary and n-state Linear Feedback Shift Registers (LFSRs)
<a href="#">20120233527</a>	Methods and Systems for Rapid Error Location in Reed-Solomon Codes
<a href="#">20120170738</a>	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders
<a href="#">20110293062</a>	Method and Apparatus for Rapid Synchronization of Shift Register Related Symbol Sequences (rapid synchronization of binary and n-state LFSRs based on received symbols)

<a href="#">20110276854</a>	Methods and Systems for Rapid Error Correction by Forward and Reverse Determination of Coding States (fast RS decoding of long sequences with single errors)
<a href="#">20110214038</a>	Methods and Systems for Rapid Error Correction of Reed-Solomon Codes (one of several applications that perform 'real-time' error location in RS code words)
<a href="#">20110182423</a>	Data Encryption and Decryption with a Key by an N-state Inverter Modified Switching Function
<a href="#">20110064214</a>	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders (applies novel adders and multiplications over GF(n))
<a href="#">20100322414</a>	TERNARY AND HIGHER MULTI-VALUE DIGITAL SCRAMBLERS/DESCRAMBLERS ( <b>issued</b> )
<a href="#">20100299579</a>	Methods and Systems for Error-Correction in Convolutional and Systematic Convolutional Decoders in Galois Configuration
<a href="#">20100271243</a>	N-State Ripple Adder Scheme Coding with Corresponding N-State Ripple Adder Scheme Decoding ( <b>issued</b> . Despite title, claims novel Feistel-like networks)
<a href="#">20100211803</a>	Multi-Valued Scrambling and Descrambling of Digital Data on Optical Disks and Other Storage Media (Despite title, claims rapid synchronization of sequences)
<a href="#">20100180097</a>	Generation and Self-Synchronizing Detection of Sequences Using Addressable Memories
<a href="#">20100164548</a>	Implementing Logic Functions With Non-Magnitude Based Physical Phenomena
<a href="#">20100109922</a>	Methods and Systems for Modifying the Statistical Distribution of Symbols in a Coded Message ( <b>issued</b> )
<a href="#">20100085802</a>	Multi-State Latches From n-State Reversible Inverters ( <b>issued</b> )
<a href="#">20090285326</a>	Generation and Detection of Non-Binary Digital Sequences (Despite title, claims novel correlation methods and apparatus)
<a href="#">20090234900</a>	Multi-Value Digital Calculating Circuits, Including Multipliers
<a href="#">20090172501</a>	Multi-State Symbol Error Correction in Matrix Based Codes
<a href="#">20090146851</a>	N-State Ripple Adder Scheme Coding with Corresponding N-State Ripple Adder Scheme Decoding ( <b>issued</b> )
<a href="#">20090138535</a>	Novel Binary and n-State Linear Feedback Shift Registers (LFSRs)
<a href="#">20090128190</a>	Implementing Logic Functions with Non-Magnitude Based Physical Phenomena
<a href="#">20090092250</a>	Methods and Systems for N-State Signal Processing with Binary Devices
<a href="#">20090077151</a>	Multi-Input, Multi-State Switching Functions and Multiplications
<a href="#">20090060202</a>	Ternary and Higher Multi-Value Digital Scramblers/Descramblers

<a href="#">20090045988</a>	Methods and Systems for Modifying the Statistical Distribution of Symbols in a Coded Message ( <b>issued</b> )
<a href="#">20080244274</a>	Methods and Systems for Processing of n-State Symbols with XOR and EQUALITY Binary Functions
<a href="#">20080180987</a>	Multi-State Latches From n-State Reversible Inverters ( <b>issued</b> )
<a href="#">20080111583</a>	IMPLEMENTING LOGIC FUNCTIONS WITH NON-MAGNITUDE BASED PHYSICAL PHENOMENA ( <b>issued</b> )
<a href="#">20080104479</a>	Symbol Error Correction by Error Detection and Logic Based Symbol Reconstruction
<a href="#">20080040650</a>	Symbol Reconstruction in Reed-Solomon Codes ( <b>issued</b> )
<a href="#">20080016432</a>	Error Correction in Multi-Valued (p,k) Codes
<a href="#">20080016431</a>	ERROR CORRECTION BY SYMBOL RECONSTRUCTION IN BINARY AND MULTI-VALUED CYCLIC CODES
<a href="#">20070258516</a>	MULTI-VALUED CHECK SYMBOL CALCULATION IN ERROR DETECTION AND CORRECTION ( <b>issued</b> )
<a href="#">20070239812</a>	Binary And N-Valued LFSR And LFCSR Based Scramblers, Descramblers, Sequence Generators and Detectors In Galois Configuration ( <b>issued</b> )
<a href="#">20070226594</a>	ERROR CORRECTING DECODING FOR CONVOLUTIONAL AND RECURSIVE SYSTEMATIC CONVOLUTIONAL ENCODED SEQUENCES ( <b>issued</b> )
<a href="#">20070208796</a>	METHODS AND APPARATUS IN FINITE FIELD POLYNOMIAL IMPLEMENTATIONS ( <b>issued</b> )
<a href="#">20070152710</a>	SINGLE AND COMPOSITE BINARY AND MULTI-VALUED LOGIC FUNCTIONS FROM GATES AND INVERTERS ( <b>issued</b> )
<a href="#">20070110229</a>	Ternary and Multi-Value Digital Signal Scramblers, Descramblers and Sequence of Generators ( <b>allowed</b> )
<a href="#">20070098160</a>	SCRAMBLING AND SELF-SYNCHRONIZING DESCRAMBLING METHODS FOR BINARY AND NON-BINARY DIGITAL SIGNALS NOT USING LFSRs
<a href="#">20070088997</a>	GENERATION AND SELF-SYNCHRONIZING DETECTION OF SEQUENCES USING ADDRESSABLE MEMORIES
<a href="#">20070071068</a>	ENCIPHERMENT OF DIGITAL SEQUENCES BY REVERSIBLE TRANSPOSITION METHODS ( <b>allowed</b> )
<a href="#">20070005673</a>	The Creation and Detection of Binary and Non-Binary Pseudo-Noise Sequences Not Using LFSR Circuits
<a href="#">20060282607</a>	Binary digital latches not using only NAND or NOR circuits ( <b>issued</b> )
<a href="#">20060187092</a>	Sequence detection by multi-valued coding and creation of multi-code sequences ( <b>issued</b> )
<a href="#">20060164883</a>	Multi-valued scrambling and descrambling of digital data on optical disks and other storage media ( <b>issued</b> )
<a href="#">20060031278</a>	Multi-value digital calculating circuits, including multipliers ( <b>issued</b> )
<a href="#">20050278661</a>	Multi-valued digital information retaining elements and memory

	devices ( <b>issued</b> )
<a href="#">20050265463</a>	Sequence detection by multi-valued coding and creation of multi-code sequences ( <b>issued</b> )
<a href="#">20050194993</a>	Single and composite binary and multi-valued logic functions from gates and inverters ( <b>issued</b> )
<a href="#">20050185796</a>	Ternary and multi-value digital signal scramblers, descramblers and sequence generators ( <b>issued</b> )
<a href="#">20050184888</a>	Generation and detection of non-binary digital sequences ( <b>issued</b> )
<a href="#">20050084111</a>	Ternary and higher multi-value digital scramblers/descramblers
<a href="#">20050053240</a>	Ternary and higher multi-value digital scramblers/descramblers