**Title:** **Reducing (a×x) + (b × y) = z in n-valued multiplication**

**Author:** **Peter Lablans, Ternarylogic LLC.**

**Date:** **May 11, 2007**

## Structure of a multiplier

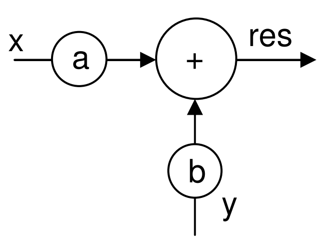
A multiplication in binary logic of two words of binary symbols is a shift-and-add operation. A multiplication in n-valued logic is unfortunately a shift-and-multiply-and-add operation. For instance one wants to n-value multiply a first word of three n-valued symbols [x y z] with a second word of n-valued symbols [a b c]. The following provides a structure of such a multiplication.

| | | | | | |
|---|---|---|---|---|---|
| word1: | | | x | y | z |
| word2: | | | a | b | c |
| | | | cx | cy | cz |
| | | bx | by | bz | |
| | ax | ay | az | | |
| result: | ax | + (bx + ay) | + (cx + by + az) | + (cy + bz) | + cz |

It should be clear that with longer words having more symbols there will be a plurality of terms like (bx + ay).

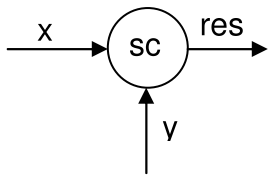
## Reducing ax + by

It is assumed that ‘a’ and ‘b’ are n-valued constants. The symbols x and y are variables which are multiplied respectively with ‘a’ and ‘b’. The expression (ax + by), wherein all elements are single n-valued symbols can be executed in its entirety by 2 circuits of which diagrams are provided below.




This circuit determines the residue ‘res’of for instance the modulo-n addition of a×x and b×y.

Assume that n = 3 and that the operations are ternary logic based. For the multipliers a = 2 and b = 2. The above diagram can then be reduced to the following diagram.




The ternary function ‘sc’ is the modulo-3 adder reduced over the ternary inverters [0 2 1] at both inputs, which are identical to a multiplier 2 modulo-3. The truth table of ‘sc’ is provided below.

| sc | | y | | |
|---|---|---|---|---|
| | res | 0 | 1 | 2 |
| x | 0 | 0 | 2 | 1 |
| | 1 | 2 | 1 | 0 |
| | 2 | 1 | 0 | 2 |

For a true multiplication also a carry has to be generated at the appropriate time. For instance 2 + 2 = 4 in decimal form. However in radix-3 (2 + 2) will provide a residue 1 and a carry 1.

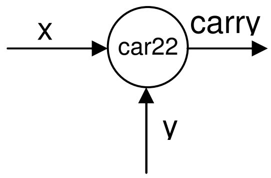
As an example it will be shown how the carry may be determined of the expression 2x + 2y in radix-3. In the following truth table the inputs to a radix-2 adder after multiplication will be shown. The result is shown in decimal form.

| dec | | 2y | | |
|---|---|---|---|---|
| | res | 0 | 2 | 4 |
| 2x | 0 | 0 | 2 | 4 |
| | 2 | 2 | 4 | 6 |
| | 4 | 4 | 6 | 8 |

In a next step, any number <3 in the truth table will be replaced by 0 (no carry). Any number < 2 <6 will be replaced by 1 and any number >5 will be replaced by a 2. This will then provide the truth table ‘car22’ for the carry of 2x + 2y.

| car22 | | y | | |
|---|---|---|---|---|
| | res | 0 | 1 | 2 |
| x | 0 | 0 | 0 | 1 |
| | 1 | 0 | 1 | 2 |
| | 2 | 1 | 2 | 2 |

The diagram for this circuit is provided below.




One can thus in one clock cycle of 2 parallel operations determine ax + by.

This approach applies to any n-valued logic implementing a radix-n arithmetic.

**About Ternarylogic LLC:** Ternarylogic LLC is a New Jersey based R&D company. Its mission is to create novel MVL technology. The company owns a portfolio of inventions related to scramblers/descramblers, sequence generators and sequence detectors, sequence correlators, gates and inverters based circuitry, non-binary multipliers, latches and other non-volatile memory elements, optical disk applications and MC-DSSS technology.

**Intellectual Property Rights**

Methods and apparatus disclosed herein are part of Ternarylogic's IP rights. Please review our portfolio.